RC5052

Programmable Synchronous DC-DC Converter for Low Voltage Microprocessors

Features

- Programmable output from 1.3V to 3.5V using an integrated 5-bit DAC
- 85% efficiency typical at full load
- Adjustable operation from 80KHz to 1MHz
- Integrated Power Good and Enable/Soft Start functions
- Overvoltage protection pin controls external SCR
- Short circuit protection with current limiting
- Drives N-channel MOSFETs
- 20 pin SOIC package
- Meets Intel Pentium II specifications using minimum number of external components
- Dead Time Adjustable

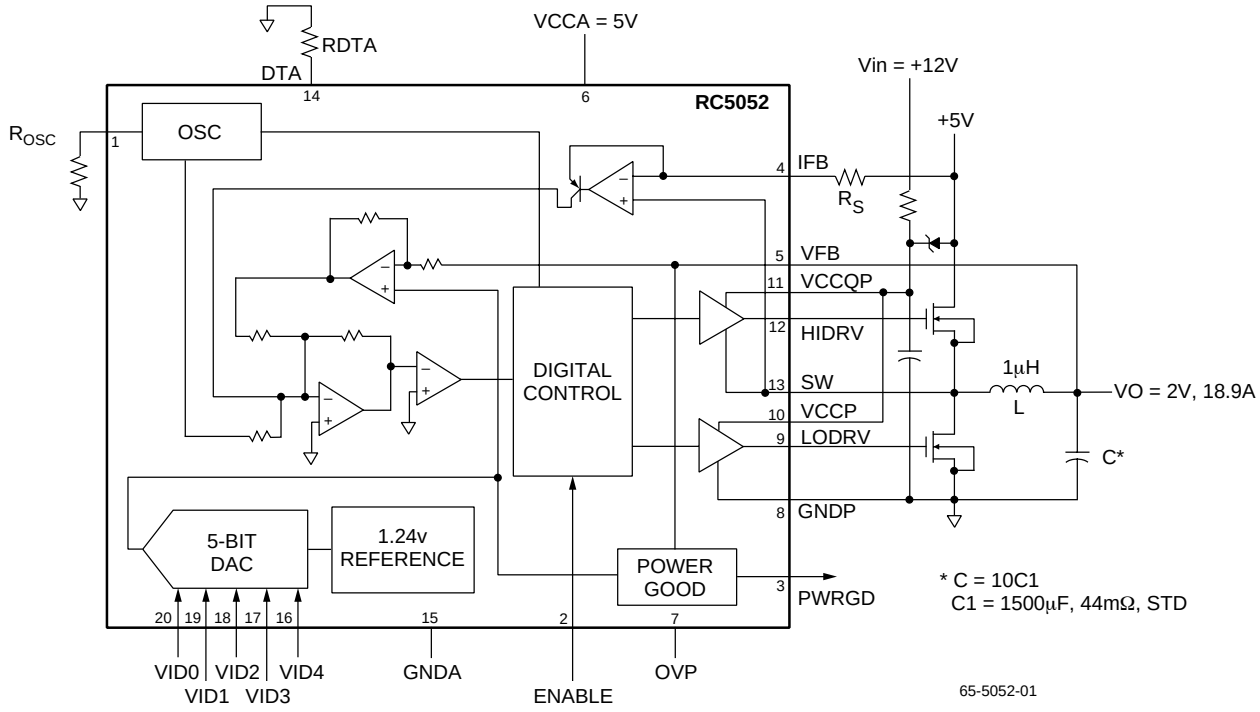
Applications

- Power supply for Pentium® II
- VRM for Pentium II processor
- Programmable step-down power supply

Description

The RC5052 is a synchronous mode DC-DC controller IC which provides an accurate, programmable output voltage for all Pentium II CPU applications. The RC5052 uses a 5-bit D/A converter to program the output voltage from 1.3V to 3.5V. The RC5052 uses a high level of integration to deliver load currents in excess of 17A from a 5V source with minimal external circuitry. Synchronous-mode operation offers optimum efficiency over the entire specified output voltage range, and the internal oscillator can be programmed from 80KHz to 1MHz for additional flexibility in choosing external components. An on-board precision low TC reference achieves tight tolerance voltage regulation without expensive external components. The RC5052 also offers integrated functions including Power Good, Output Enable/ Soft Start , over-voltage protection and current limiting.

Block Diagram



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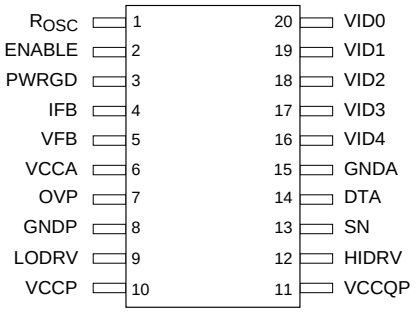
Rev. 0.9.7

Pin Assignments



Pin Definitions

Pin Number	Pin Name	Pin Function Description
14	DTA	**Dead Time Adjust.** This pin allows control over dead time via an external resistor.
2	ENABLE	**Output Enable.** A logic LOW on this pin will disable the output. An internal current source allows for open collector. A 2.5nF soft start capacitor should be connected from this pin to ground.
15	GNDA	**Analog Ground.** Return path for low power analog circuitry. This pin should be connected to a low impedance system ground plane to minimize ground loops.
8	GNDP	**Power Ground.** Return pin for high currents flowing in pin 10 (VCCP). Connect to a low impedance ground.
12	HIDRV	**High Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET. The trace from this pin to the MOSFET gate should be < 0.5".
4	IFB	**Current Feedback.** Pins 4 is used, in conjunction with pin 14, SW, as the input for the current feedback control loop. Layout of these trace is critical to system performance. See Application Information for details.
9	LODRV	**Low Side FET Driver.** Connect this pin to the gate of an N-channel MOSFET for synchronous operation. The trace from this pin to the MOSFET gate should be < 0.5".
7	OVP	**Over Voltage Protection.** This pin triggers the gate of an external SCR.
3	PWRGD	**Power Good Flag**. An open collector output that will be at logic LOW if the output voltage is not within ±12% of the nominal output voltage setpoint.
1	ROSC	**Oscillator Resistor Connection.** Connecting an external resistor to this pin sets the internal oscillator frequency. Layout of this pin is critical to system performance. See Application Information for details.
13	SW	**High side driver source and low side driver drain switching node.** Together with IFB pin allows sensefet implementation. This is also the high current return for pin 11 (VCCQP).
6	VCCA	**Analog VCC.** Connect to system 5V supply and decouple with a 0.1μF ceramic capacitor.
10	VCCP	**Power VCC for Low Side Driver Fet.** Connect to system 12V supply and place a 4.7μF Tantalum capacitor for decoupling and local charge storage.
11	VCCQP	**Power VCC.** This is the supply for the high side FET driver. VCCQP must be connected to a voltage of at least VCCA + $V_{GS,ON}$ (MOSFET) + 1 volt.
5	VFB	**Voltage Feedback.** Pin 5 is used as the input for the voltage feedback control loop and as the low side current feedback input. See Application Information for details regarding correct layout.
17-20	VID0-VID3	**Voltage Identification Code Inputs.** These open collector/TTL compatible inputs will program the output voltage over the ranges specified in Table 1. Pull-up resistors are internal to the controller.
16	VID4	**VID4 Input.** A logic 1 on this open collector/TTL input will enable the VID3–VID0 inputs to set the output from 2.1V to 3.5V, and a logic 0 will set the output from 1.3V to 2.05V, as shown in Table 1. Pullup resistors are internal to the controller.

Preliminary Information

Absolute Maximum Ratings

Input Voltage, Vin	13V
Supply Voltages, VCCA, VCCP, VCCQP (DC)	13V
Supply Voltage VCCQP, Charge PUMP (Vin + VCCA)	18V
Voltage Identification Code Inputs, VID4-VID0	5V
Junction Temperature, T_J	150°C
Storage Temperature	-65 to 150°C
Lead Soldering Temperature, 10 seconds	300°C

Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage, VCCA, VCCP		4.75	5	5.25	V
Input Logic HIGH		2.0			V
Input Logic LOW				0.8	V
Ambient Operating Temp		0		70	°C
Output Driver Supply, VCCQP, VCCP		9.5		12	V
PWRGD threshold	Logic High Logic Low	93 88		107 112	$\%V_O$ $\%V_O$

Electrical Specifications

(V_{CCA} = 5V, V_{CCP} & V_{CCQP} = 12V, V_{OUT} = 2.8V, f_{osc} = 300 KHz, and T_A = +25˚C using circuit in Figure 1, unless otherwise noted) The • denotes specifications which apply over the full operating temperature range.

Parameter	Conditions		Min.	Typ.	Max.	Units
Output Voltage	See VRM Spec 8.2, Rev 0.6	•	1.8		3.5	V
Output Current	See VRM Spec 8.2, Rev 0.6		0.04		18.9	A
Initial Voltage Setpoint	Minimum I_{LOAD}			±10		mV
Output Temperature Drift	T_A = 0 to 60°C	•		+10		mV
Line Regulation	V_{IN} = 4.75V to 5.25V	•		±2		mV
Output Ripple	20 MHz BW, Max I_{LOAD}			±11		mV
Output Voltage (Pentium II)	VRM 8.2 Specification Rev 0.6: 2.8V -60/+100mV, R_S = TBD					
Steady State	Minimum Load[1] (See Table 1)	•	2.834		2.90	V
Steady State	Maximum Load[1] (See Table 1)	•	2.74		2.806	V
Negative Transient (Min to Max Load)	300MHz Pentium II	•	2.67			V
Positive Transient (Max to Min Load)	300MHz Pentium II	•			2.93	V
Load Regulation (Droop)	I_{LOAD} = Minimum to Maximum Current	•			-104	mV
Output Voltage (Deschutes)	VRM 8.2 Specification Rev. 0.6: 2V±60mV All but 266/333MHz (-60/+100mV), R_S = TBD					
Steady State	Minimum Load[1] (See Table 1)	•	2.01		2.06	V
Steady State	Maximum Load[1] (See Table 1)	•	1.94		1.99	V
Steady State	Minimum Load (266MHz and 333MHz)	•	2.05		2.10	V
Negative Transient (Min to Max Load)	450MHz Deschutes	•	1.90			V
Positive Transient (Max to Min Load)	450MHz Deschutes	•			2.10	V
Negative Transient (Min to Max Load)	Flexible Motherboard	•	1.87			V
Positive Transient (Max to Min Load)	Flexible Motherboard	•			2.13	V

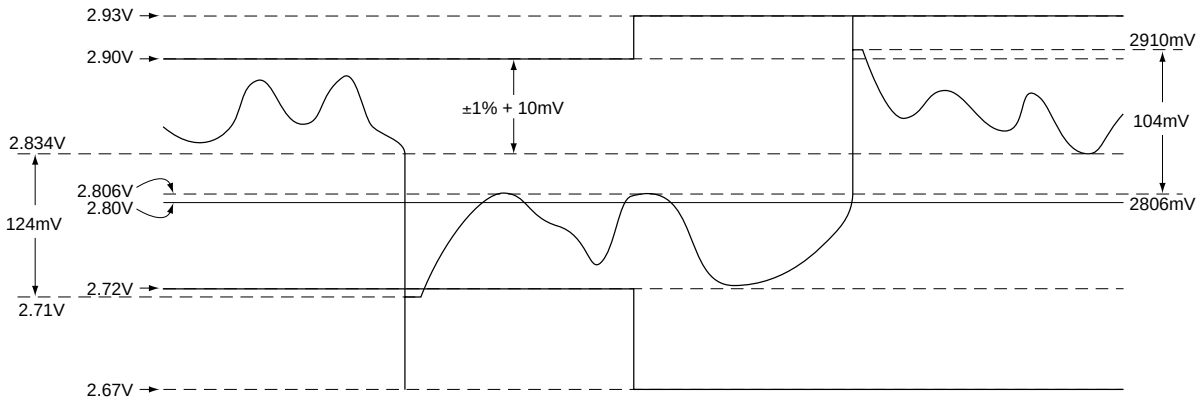
Preliminary Information

Parameter	Conditions		Min.	Typ.	Max.	Units
Load Regulation (Droop) @ 2V	I_{LOAD} = Minimum to Maximum Current				-80	mV
Short Circuit Detect Threshold		•		TBD		mV
Efficiency	Maximum Load	•	80	85		%
Output Driver Rise and Fall Time	See Figure 2			50		ns
Output Driver Nonoverlap Time	See Adjustability			50		ns
Turn-on Response Time	Minimum to Maximum Current				10	ms
Oscillator Range			80	300	1000	KHz
Oscillator Frequency	R_{OSC} = 80K		270	300	330	KHz
Maximum Duty Cycle			90	95		%

Note:
1. Figures 1 and 2 are an illustration of the voltage specifications in static and transient mode.

Table 1. Processor Load and Slew Rate

	PII	Deschutes 450MHz	Deschutes Flexible Motherboard
Maximum Load	14.2A	14.2A	18.9A
Minimum Load	0.2A	40mA	40mA
Slew Rate	30A/μs	20A/μs	20A/μs



$-\Delta V = 2834 - 2710 = 124mV$
$+\Delta V = 2910 - 2806 = 104mV$

Figure 1. Pentium II Static and Transient Specification Illustration (droop saves 3C1, from 11 down to 8 capacitors)

Preliminary Information

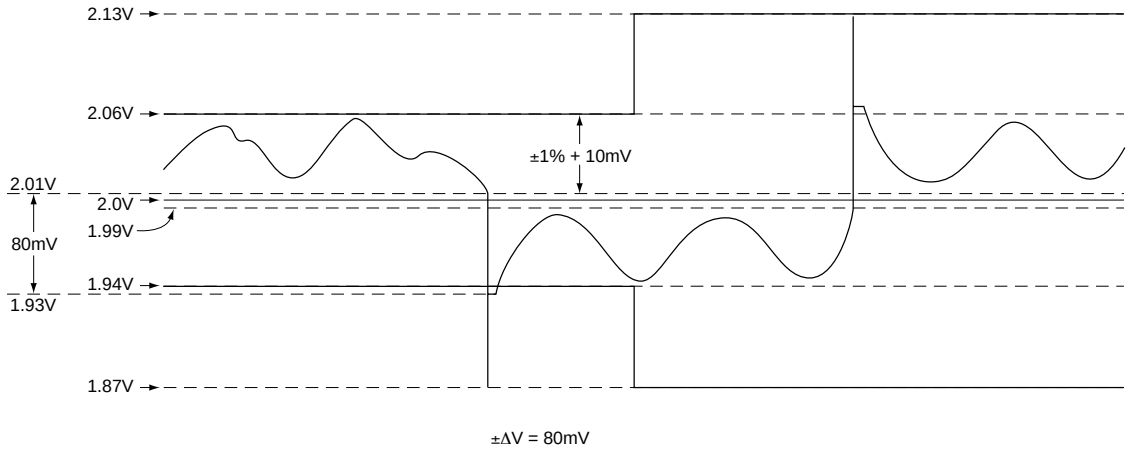


Figure 2. Flexible Motherboard Static and Transient Specification Illustration (droop saves 4C1 from 14 down to 10)

Applications Discussion

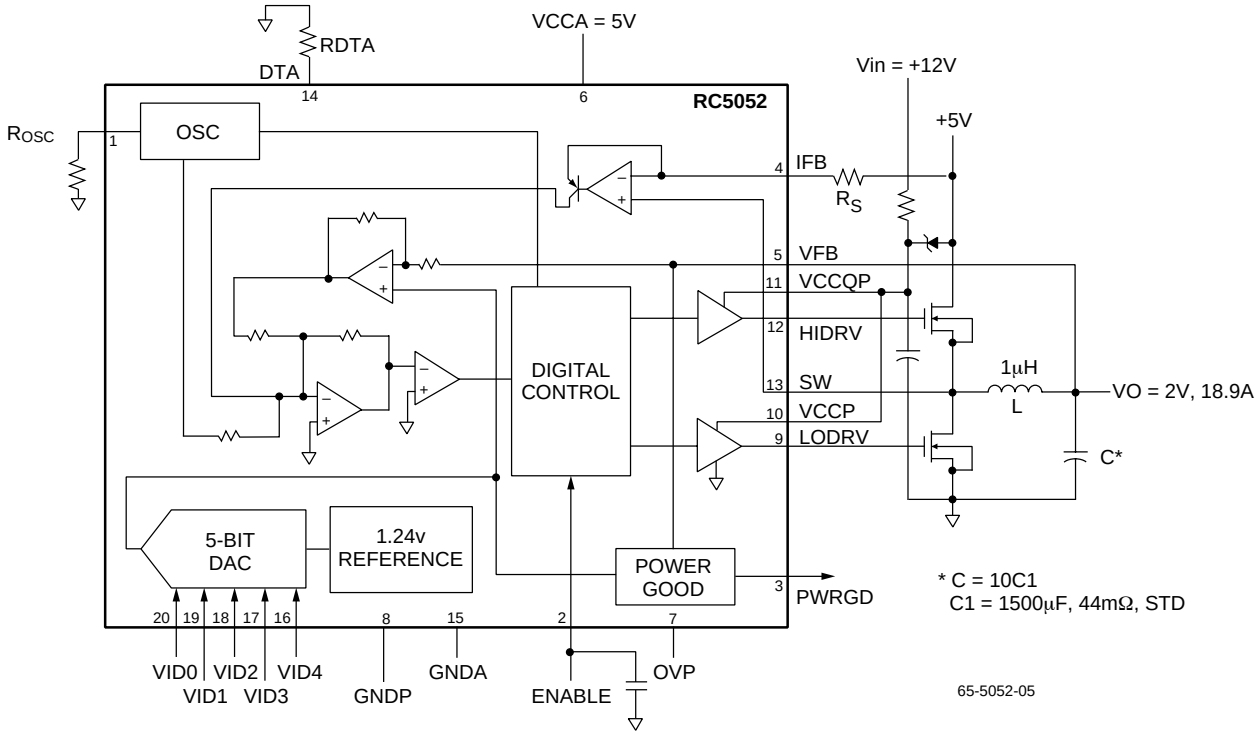


Figure 3. Desktop Application

Preliminary Information

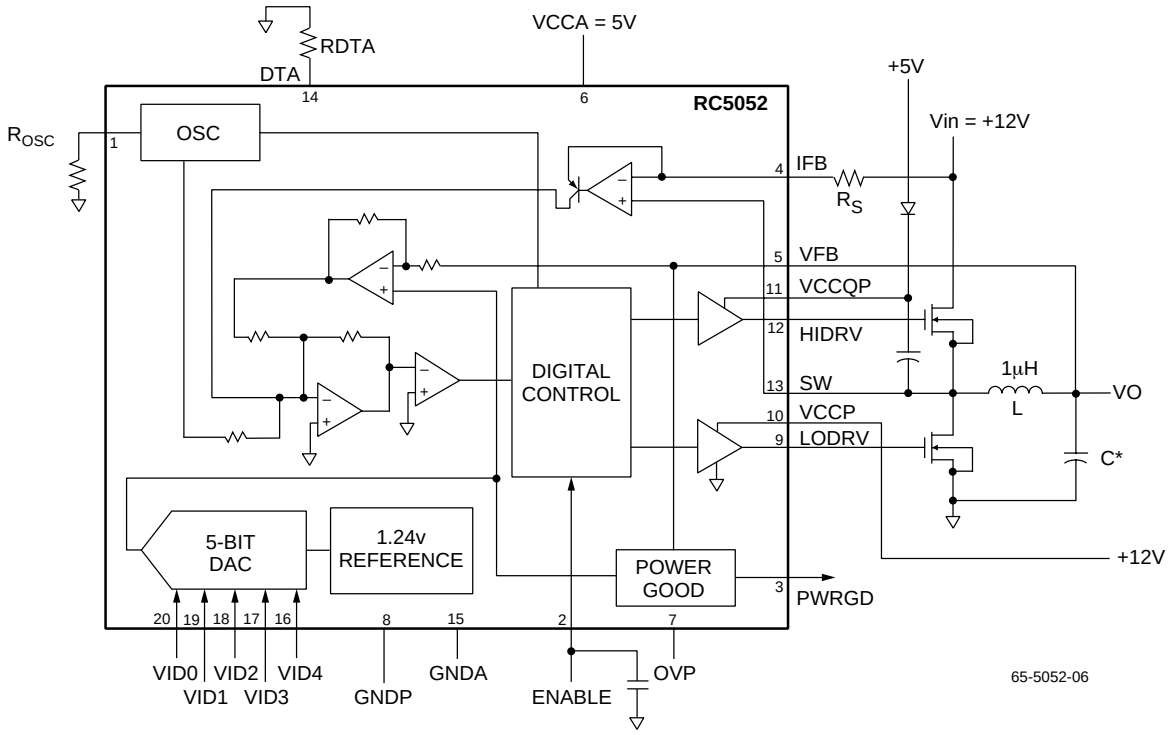


Figure 4. Server Application

Table 2. Output Voltage Programming Codes

PIN NAME					NOMINAL OUTPUT VOLTAGE DACOUNT	PIN NAME					NOMINAL OUTPUT VOLTAGE DACOUNT
VID4	VID3	VID2	VID1	VID0		VID4	VID3	VID2	VID1	VID0	
0	1	1	1	1	1.30	1	1	1	1	1	2.0
0	1	1	1	0	1.35	1	1	1	1	0	2.1
0	1	1	0	1	1.40	1	1	1	0	1	2.2
0	1	1	0	0	1.45	1	1	1	0	0	2.3
0	1	0	1	1	1.50	1	1	0	1	1	2.4
0	1	0	1	0	1.55	1	1	0	1	0	2.5
0	1	0	0	1	1.60	1	1	0	0	1	2.6
0	1	0	0	0	1.65	1	1	0	0	0	2.7
0	0	1	1	1	1.70	1	0	1	1	1	2.8
0	0	1	1	0	1.75	1	0	1	1	0	2.9
0	0	1	0	1	1.80	1	0	1	0	1	3.0
0	0	1	0	0	1.85	1	0	1	0	0	3.1
0	0	0	1	1	1.90	1	0	0	1	1	3.2
0	0	0	1	0	1.95	1	0	0	1	0	3.3
0	0	0	0	1	2.00	1	0	0	0	1	3.4
0	0	0	0	0	2.05	1	0	0	0	0	3.5

NOTE: 0 = connected to GND or V_{SS} 1 = OPEN

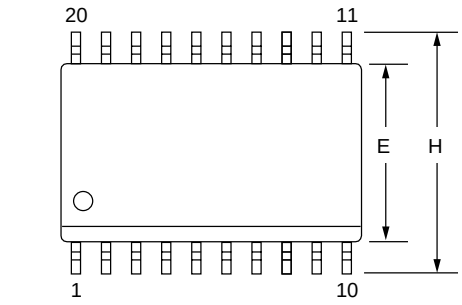
Mechanical Dimensions

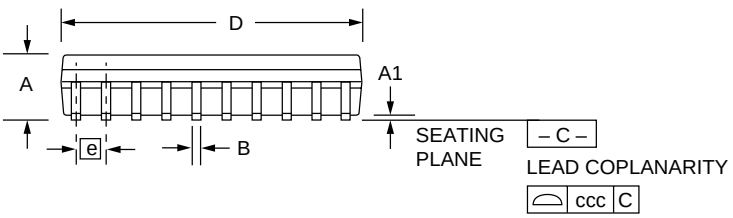
20 Lead SOIC

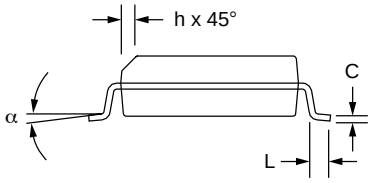
Symbol	Inches		Millimeters		Notes
	Min.	Max.	Min.	Max.	
A	.093	.104	2.35	2.65	
A1	.004	.012	0.10	0.30	
B	.013	.020	0.33	0.51	
C	.009	.013	0.23	0.32	5
D	.496	.512	12.60	13.00	2
E	.291	.299	7.40	7.60	2
e	.050 BSC		1.27 BSC		
H	.394	.419	10.00	10.65	
h	.010	.029	0.25	0.75	
L	.016	.050	0.40	1.27	3
N	20		20		6
α	0°	8°	0°	8°	
ccc	—	.004	—	0.10	

Notes:

1. Dimensioning and tolerancing per ANSI Y14.5M-1982.
2. "D" and "E" do not include mold flash. Mold flash or protrusions shall not exceed .010 inch (0.25mm).
3. "L" is the length of terminal for soldering to a substrate.
4. Terminal numbers are shown for reference only.
5. "C" dimension does not include solder finish thickness.
6. Symbol "N" is the maximum number of terminals.







Preliminary Information

Ordering Information

Product Number	Package
RC5052M	20 Lead SOIC

Preliminary Information

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